

WEST

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L8 and predict\$3 and fail\$3

1

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side by side

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result set

DB=USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ

<u>L9</u>	L8 and predict\$3 and fail\$3	1	<u>L9</u>
<u>L8</u>	L7 and (ris\$3 or fall\$3) with time	3	<u>L8</u>
<u>L7</u>	L6 and pulse with width	6	<u>L7</u>
<u>L6</u>	L1 and AC with parametric\$4 with test\$3	40	<u>L6</u>
<u>L5</u>	L2 and signal same input	5	<u>L5</u>
<u>L4</u>	L2 and control\$5 same input	4	<u>L4</u>
<u>L3</u>	L2 and control\$5 with input	4	<u>L3</u>
<u>L2</u>	L1 and pulse ADJ width and predict\$3 with failure	5	<u>L2</u>
<u>L1</u>	(IC or integrated circuit) and test\$3 with signal	17630	<u>L1</u>

END OF SEARCH HISTORY

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L16 and ((324/\$)!CCLS.)

5

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Database:**Search:**

L17

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<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
side by side		result set	
<i>DB=USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ</i>			
<u>L17</u>	L16 and ((324/\$)! .CCLS.)	5	<u>L17</u>
<u>L16</u>	L15 and fail\$3	32	<u>L16</u>
<u>L15</u>	L14 and (BIST or built-in)	46	<u>L15</u>
<u>L14</u>	IC with test\$3 and pulse with width and (ris\$3 or fall\$3) with time	146	<u>L14</u>
<u>L13</u>	L11 and (ris\$3 or fall\$3) with time	0	<u>L13</u>
<u>L12</u>	L11 and pulse with width	0	<u>L12</u>
<u>L11</u>	L10 and generat\$3 with signal	1	<u>L11</u>
<u>L10</u>	5457400.pn.	1	<u>L10</u>
<u>L9</u>	L8 and predict\$3 and fail\$3	1	<u>L9</u>
<u>L8</u>	L7 and (ris\$3 or fall\$3) with time	3	<u>L8</u>
<u>L7</u>	L6 and pulse with width	6	<u>L7</u>
<u>L6</u>	L1 and AC with parametric\$4 with test\$3	40	<u>L6</u>
<u>L5</u>	L2 and signal same input	5	<u>L5</u>
<u>L4</u>	L2 and control\$5 same input	4	<u>L4</u>
<u>L3</u>	L2 and control\$5 with input	4	<u>L3</u>
<u>L2</u>	L1 and pulse ADJ width and predict\$3 with failure	5	<u>L2</u>
<u>L1</u>	(IC or integrated circuit) and test\$3 with signal	17630	<u>L1</u>

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L2 and signal same input

5

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L5	Refine Search
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result set*DB=USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ*

<u>L5</u>	L2 and signal same input	5	<u>L5</u>
<u>L4</u>	L2 and control\$5 same input	4	<u>L4</u>
<u>L3</u>	L2 and control\$5 with input	4	<u>L3</u>
<u>L2</u>	L1 and pulse ADJ width and predict\$3 with failure	5	<u>L2</u>
<u>L1</u>	(IC or integrated circuit) and test\$3 with signal	17630	<u>L1</u>

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